74HC595

8-Bit Shift Registers W ith Latched 3-State Output

GENERAL DESCRIPTION

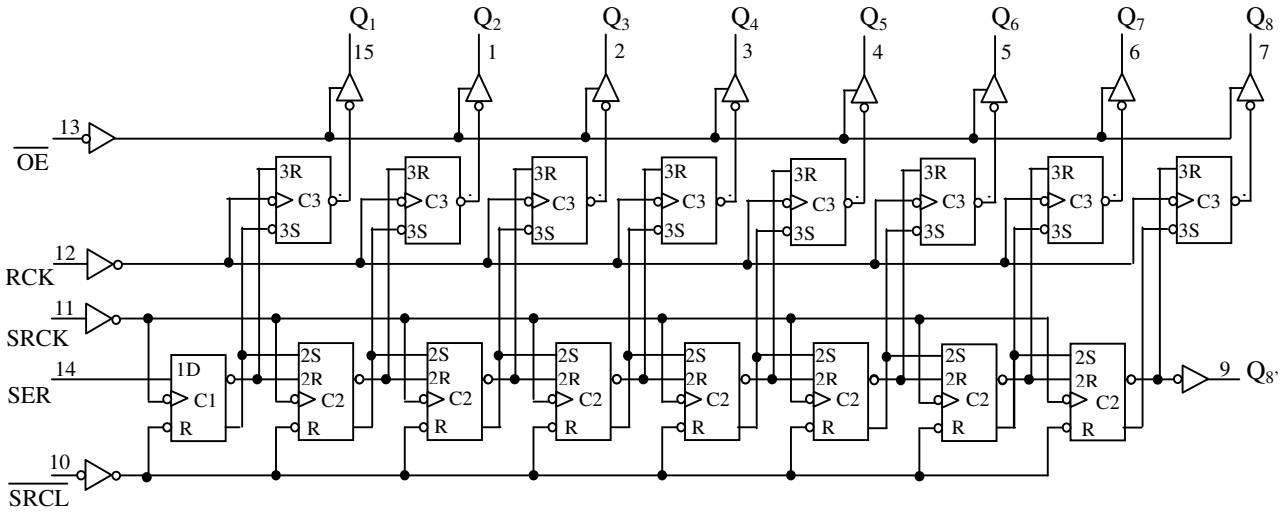
74HC595 is fabricated with high-speed silicon gate CMOS technology. It contains an 8-bit serial-in, serial or parallel-out shift register and an 8-bit D-type storage register with parallel 3-state outputs. The shift and storage register have independent clock inputs. Both the shift register clock (SRCK) and storage register clock (RCK) are positive-edge triggered.

The shift register has a direct overriding clear input ($\overline{\text{SRCL}}$), serial data input (SER), and serial outputs for cascading. When the output-enable ($\overline{\text{OE}}$) input is high, the outputs are in the high-impedance state. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

FEATURES

- 8-bit serial-in, parallel-out shift register with storage
- Shift register has direct clear
- 8-bit D-type storage register with parallel 3-state outputs
- Two independent clocks for shift and storage register
- Wide operating power supply voltage 2-6V
- Low input current < 1μA
- Low power consumption, Max. 80μA (74HC595)
- Output driving capacity ± 6 mA at 5V
- Typical propagation delay 13nS

LOGIC DIAGRAM



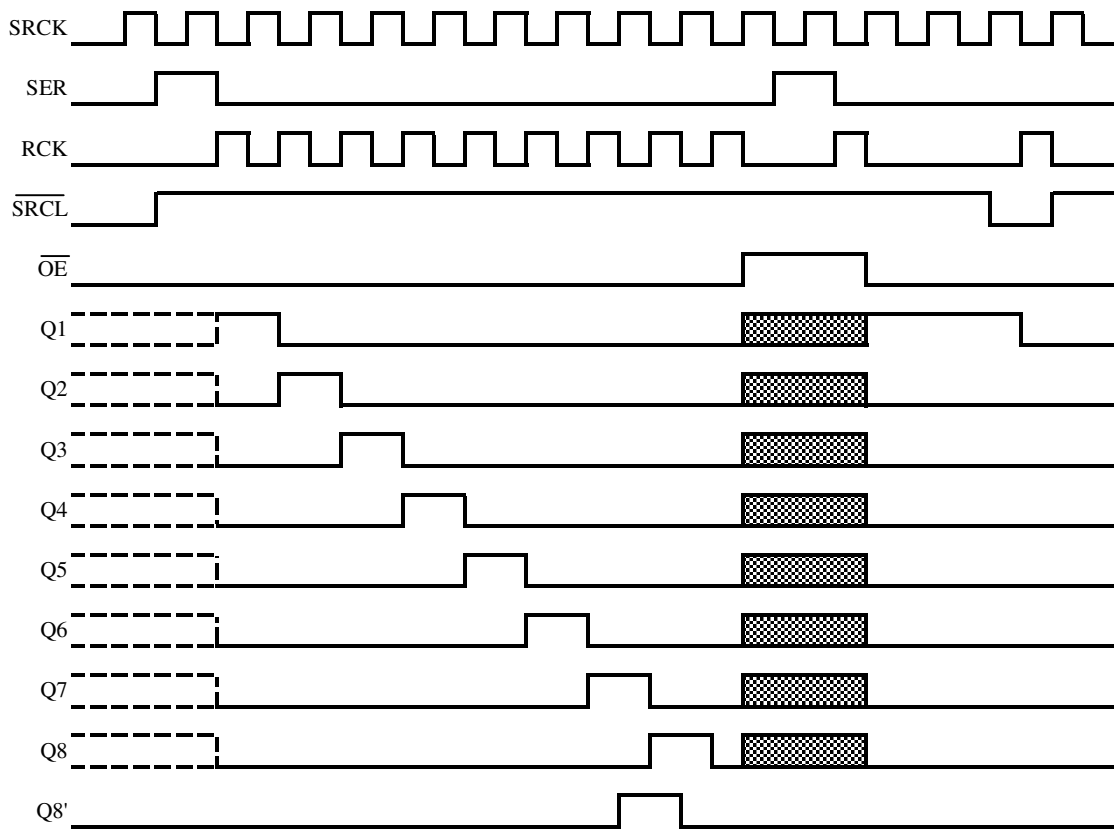
FUNCTIONAL DESCRIPTION

1. Truth Table

Inputs					Function
SER	SRCK	$\overline{SRCL}$	RCK	$\overline{OE}$	
X	X	X	X	H	Outputs Q1-Q8 are disabled.
X	X	X	X	L	Outputs Q1-Q8 are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored in the latch.

H = High Level (steady state). L= Low Level (steady state)
X = Irrelevant (don't care)
↑ = Transition from low to high level.

2. Logic Waveform



Note: ▩ implies that the outputs are in 3-state mode.

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
DC supply voltage Vcc	- 0.5 ~ + 7.0	V
DC input clamp current Iik (Vi<0 or Vi>Vcc)	±20	mA
DC output clamp current Iok (Vo<0 or Vo>Vcc)	±20	mA
DC Current Drain per pin, any output (I_{out})	±35	mA
DC supply Current, Vcc or GND (Icc)	±70	mA
Storage Temperature(T_{STG})	-65 ~ +150	℃
Lead Temperature(T_L) (Soldering, 10seconds)	260	℃

Note:

1. Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

RECOMMENDED OPERATING CONDITONS

Parameter		Min.	Normal	Max.	Unit
Power Supply Voltage (Vcc)		2	5	6	V
V_{IH} High-level input voltage	VCC=2.0V	1.5			V
	VCC=4.5V	3.15			
	VCC=6.0V	4.2			
V_{IL} Low-level Input Voltage	VCC=2.0V			0.5	V
	VCC=4.5V			1.35	
	VCC=6.0V			1.8	
V_I Input Voltage		0		Vcc	V
V_O Output Voltage		0		Vcc	V
Operating Temperature (TA)	74HC595	-40		85	℃
Input Rise/Fall Times (tr, tf)	VCC=2.0V			1000	ns
	VCC=4.5V			500	
	VCC=6.0V			400	

Note:

2. All unused inputs of the device must be held at Vcc or GND to ensure proper device operation.
3. If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and Vcc = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

DC ELECTRICAL CHARACTERISTICS

(Apply across temperature range unless otherwise specified)

PARAMETER	TEST CONDITIONS		Vcc	TA = 25℃ MIN	TYP	MAX	54HC595 74HC595 MIN	MAX	UNIT
V_{OH}	V_I= V_{IH} or V_{IL}	I_{OH} = -20uA	2 V	1.9	1.998		1.9		V
			4.5V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		I_{OH} = -6 mA	4.5V	3.98	4.3		3.84		
		I_{OH} = -7.8mA	6 V	5.48	5.8		5.34		
V_{OL}	V_I= V_{IH} or V_{IL}	I_{OL} =20uA	2 V		0.002	0.1		0.1	V
			4.5V		0.001	0.1		0.1	
			6 V		0.001	0.1		0.1	
		I_{OL} = 6mA	4.5V		0.17	0.26		0.33	
		I_{OL} =7.8mA	6 V		0.15	0.26		0.33	
I_I	V_I = Vcc or 0		6 V		±0.1	±100		±1000	nA
I_{OZ}	V_O = Vcc or 0, Q1-Q8		6 V		±0.01	±0.5		±5	uA
Icc	V_I = Vcc or 0 I_O = 0		6 V			8		80	uA
Ci			2V ~ 6V		3	10		10	pF

TIMING REQUREMENTS OVER RECOMMENED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

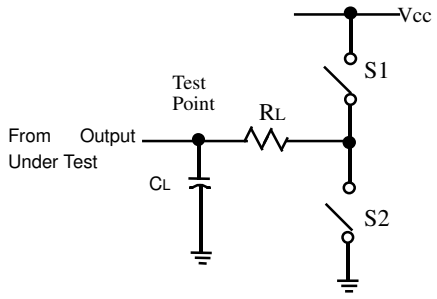
Parameter	Symbol	Unit	Guaranteed Limit TA=25℃	-40~+85	Test Condition	
Clock frequency	f_{clock}	MHz	6	5	Vcc=2.0V	
			31	25	Vcc=4.5V	
			36	29	Vcc=6.0V	
Pulse duration	tw	ns	80	100	Vcc=2.0V	SRCK or LCK high or low
			16	20	Vcc=4.5V	
			14	17	Vcc=6.0V	
			80	100	Vcc=2.0V	$\overline{\text{SRCL}}$ low
			16	20	Vcc=4.5V	
			14	17	Vcc=6.0V	
Setup time	tsu	ns	100	125	Vcc=2.0V	SER before SRCK ↑
			20	25	Vcc=4.5V	
			17	21	Vcc=6.0V	
			75	94	Vcc=2.0V	SRCK ↑ before LCK ↑ (Note 4)
			15	19	Vcc=4.5V	
			13	16	Vcc=6.0V	
			50	65	Vcc=2.0V	$\overline{\text{SRCL}}$ low before RCK ↑
			10	13	Vcc=4.5V	
			9	11	Vcc=6.0V	
			50	60	Vcc=2.0V	SRCL high(inactive) before SRCK ↑
			10	12	Vcc=4.5V	
			9	11	Vcc=6.0V	
Hold time,	th	ns	0	0	Vcc=2~6V	SER after SRCK ↑

Note: . 4. This setup time allows the latch to receive stable data from the shift register. The clock can be connected together, in this case the shift register is one clock pulse ahead of the latch.

AC ELECTRICAL CHARACTERISTICS (unless otherwise noted)

Parameter	Symbol	From (Input)	To (Output)	Unit	Vcc	Ta = 25℃ Min	Typ	Max	74HC595 Min	Max	Parameter
Maximum clock frequency	fmax			MHz	2V	6	26		5		CL=50pF
					4.5V	31	38		25		
					6V	36	42		29		
Maximum Propagation Delay (Clock to Q)	tpd	SRCK	Q8'	ns	2V		50	160		200	CL=50pF
					4.5V		17	32		40	
					6V		14	27		34	
		LCK	Q1-Q8	ns	2V		50	150		187	
					4.5V		17	30		37	
					6V		14	26		32	
		LCK	Q1-Q8	ns	2V		60	200		250	CL=150pF
					4.5V		22	40		50	
					6V		19	34		43	
Maximum Propagation Delay (SRCL to Q8'	tPHL	$\overline{SRCL}$	QH'	ns	2V		51	175		219	CL=50pF
					4.5V		18	35		44	
					6V		15	30		37	
Maximum Propagation Delay ($\overline{OE}$ to Q)	ten	$\overline{OE}$	Q1-Q8	ns	2V		40	150		187	CL=50pF
					4.5V		15	30		37	
					6V		13	26		32	
					2V		70	200		250	CL=150pF
					4.5V		23	40		50	
					6V		19	34		43	
	tdis	$\overline{OE}$	Q1-Q8	ns	2V		42	200		250	CL=50pF
					4.5V		23	40		50	
					6V		20	34		43	
Maximum Output Rising and Falling Time	tt		Q1-Q8	ns	2V		28	60		75	CL=50pF
					4.5V		8	12		15	
					6V		6	10		13	
			Q8'		2V		28	75		95	
					4.5V		8	15		19	
					6V		6	13		16	
			Q1-Q8		2V		45	210		265	CL=150pF
					4.5V		17	42		53	
					6V		13	36		45	
Power Dissipation Capacitance	CPD			pF			400		–	–	

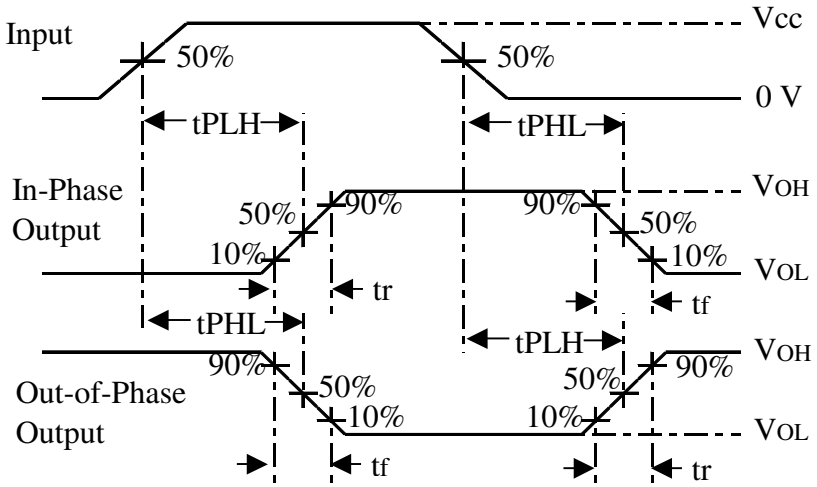
PARAMETER MEASUREMENT INFORMATION



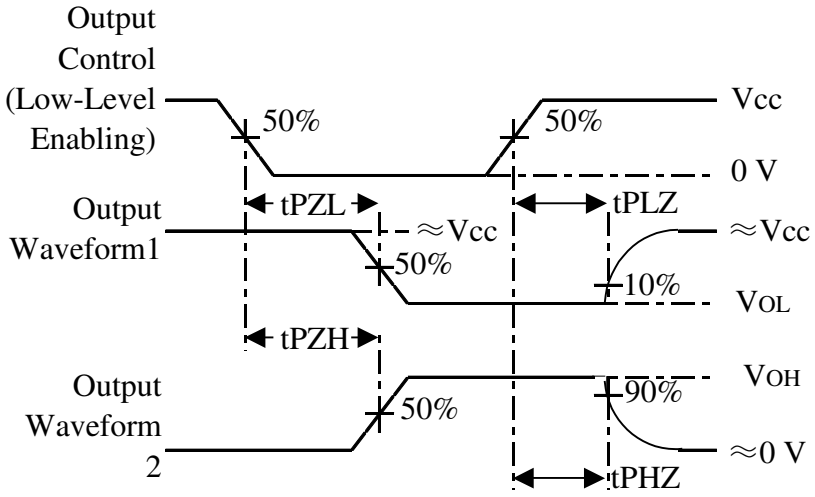
PARAMETER		RL	CL	S1	S2
ten	tPZH	1 kΩ	50 pF or 150 pF	Open	Closed
	tPZL			Closed	Open
tdis	tPHZ	1k Ω	50 pF	Open	Closed
	tPLZ			Closed	Open
tpd or tt		-	50 pF or 150 pF	Open	Open

AC SWITCHING WAVEFORM AND AC TEST CIRCUIT

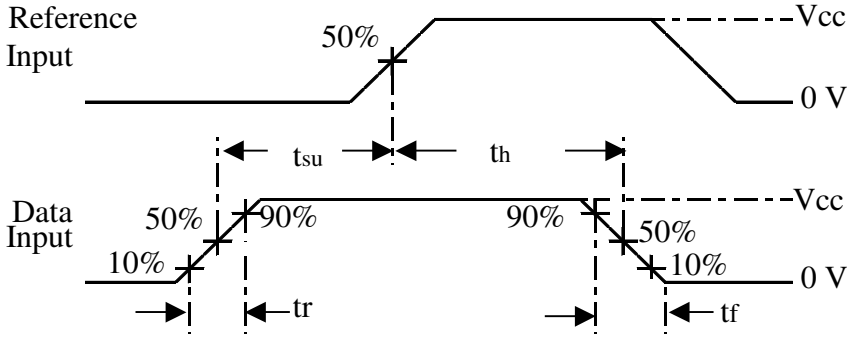
Voltage Waveforms 1. Propagation Delay and Output Transition Times



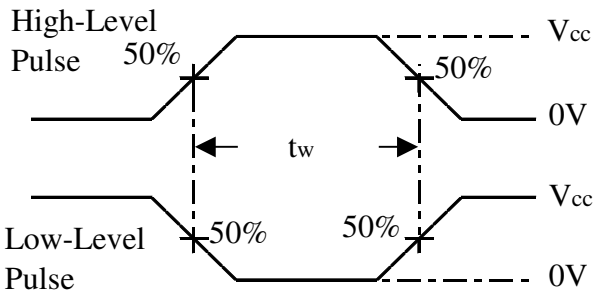
Voltage waveforms 2. Enable And Disable Times For 3-State Outputs



Voltage waveforms 3. Setup And Hold and Input Rise And Fall Times



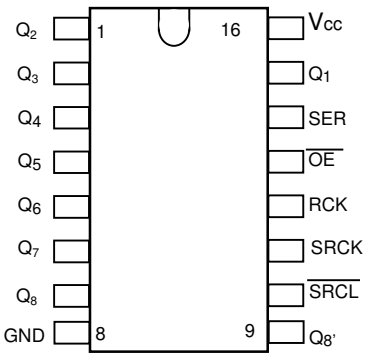
Voltage waveforms 4. Pulse Durations



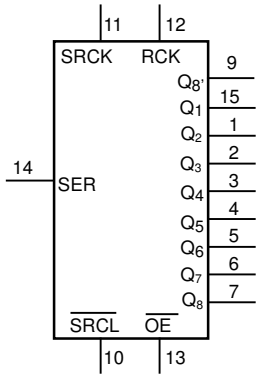
Note:
5. C_L includes probe and test-fixture capacitance.
6. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω, tr = 6 ns, tf = 6 ns.
7. For clock inputs, fmax is measured when the input duty cycle is 50%.
8. The outputs are measured one at a time, with one input transition per measurement.
9. tPLZ and tPHZ are the same as tdis.
10. tPZL and tPZH are the same as ten.
11. tPLH and tPHL are the same as tpd.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
15, 1, 2, 3, 4, 5, 6, 7	$Q_1 – Q_8$	Parallel data outputs
9	Q_8'	Serial data output
10	$\overline{SRCL}$	Shift register reset input (active low)
11, 12	SRCK, RCK	Shift and storage register clock inputs (triggered at positive edge)
13	$\overline{OE}$	Output enable input (active low)
14	SER	Serial data input
8	GND	Ground (0V)
16	V_{CC}	Positive power supply

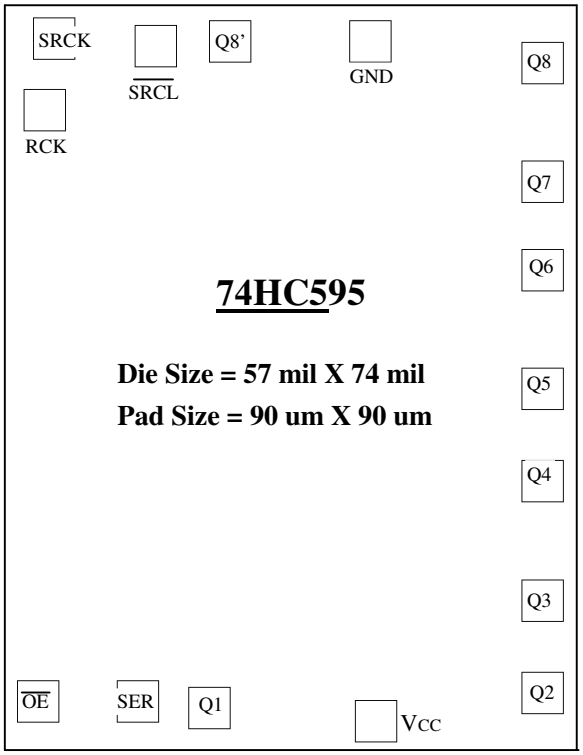


Pin Configuration



Logic Symbol

PAD DIAGRAM



The Coordinate of Each Pad

$\overline{OE}$	(-615.1, -748.2)	Q6	(479.8, 185.0)
SER	(-398.1, -748.2)	Q7	(479.8, 379.6)
Q1	(-243.3, -762.4)	Q8	(479.8, 635.4)
VCC	(118.3, -789.2)	GND	(105.8, 683.3)
Q2	(479.8, -714.6)	Q8'	(-199.4, 683.3)
Q3	(479.8, -520.6)	$\overline{SRCL}$	(-359.7, 673.2)
Q4	(479.8, -264.8)	SRCK	(-581.0, 689.2)
Q5	(479.8, -70.2)	RCK	(-600.9, 534.4)

Note: Substrate should be connected to Vcc or left it open.